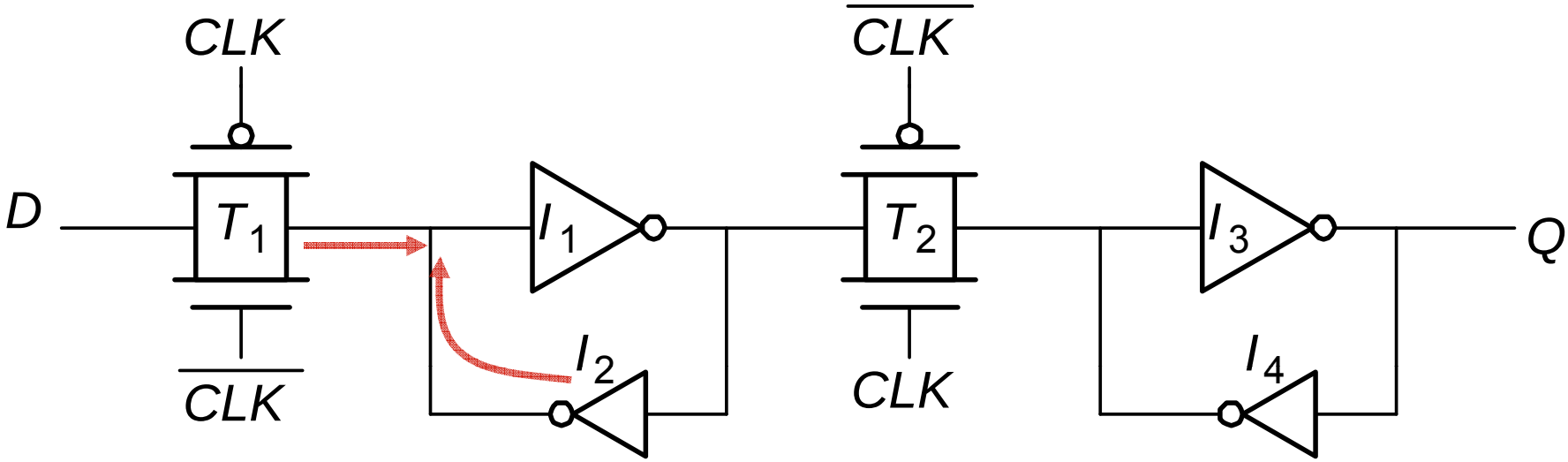
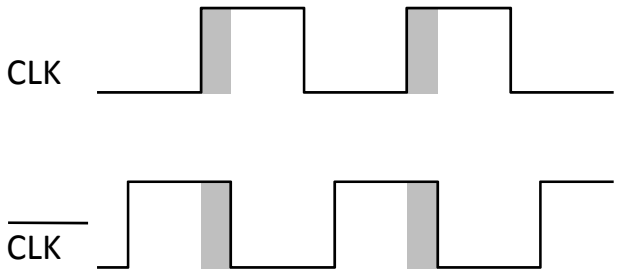
ECE680: Physical VLSI Design

Chapter V

Implementation Strategies for Digital ICs
Part 2: Issues of Logic Gates

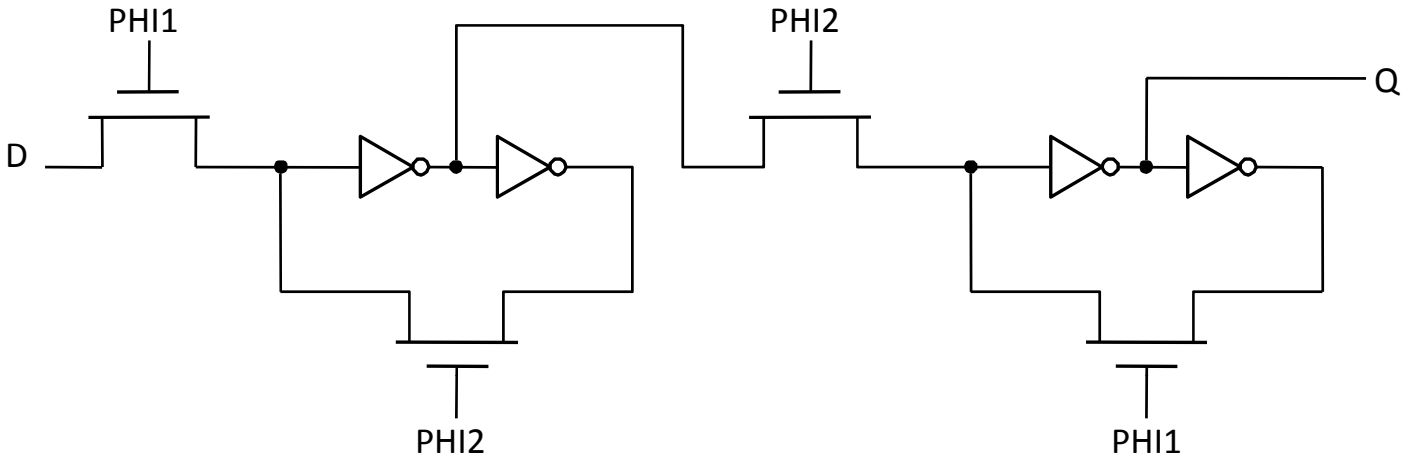
Clock Overlap and Race Condition



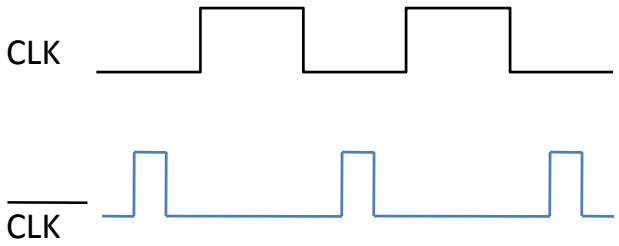


Overlapping clock pairs (1,1) and (0,0)

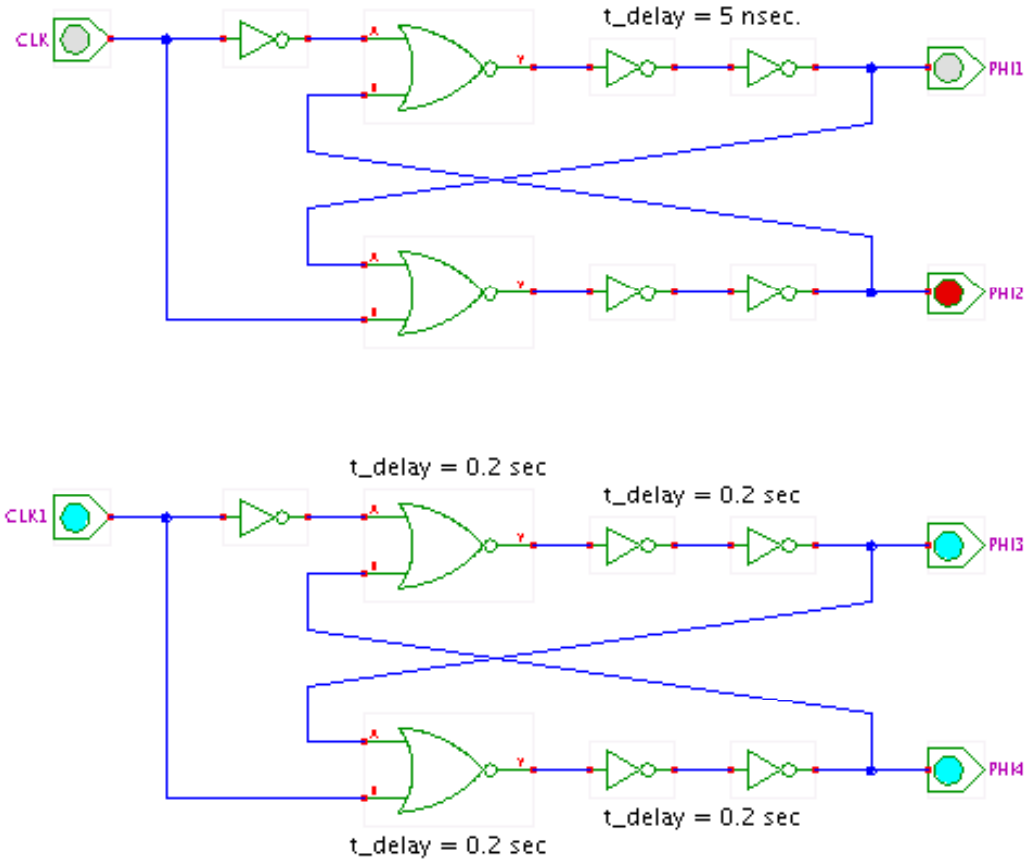
Avoid Clock Overlap



nMOS FF with nonoveralp (high) clocks PHI1 and PHI2



Avoid Clock Overlap

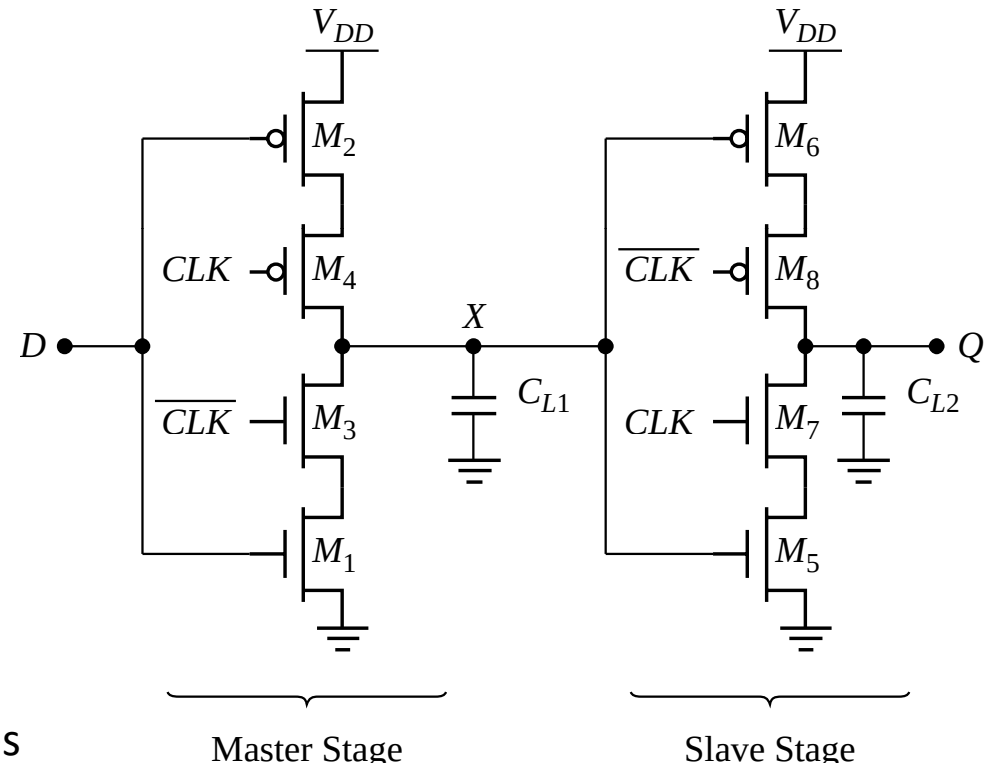


Avoid Clock Overlap

Insensitive to CLK and $\overline{CLK}$ overlap

» Prevents a change on D from affecting Q during overlap

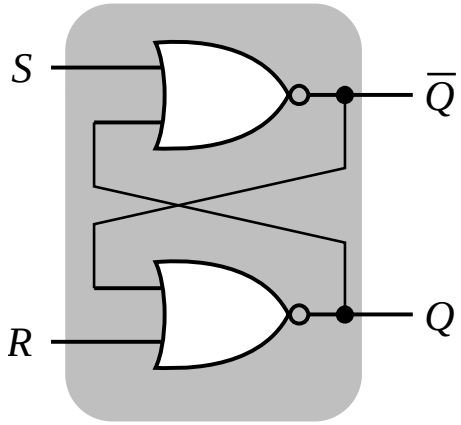
Clock CMOS

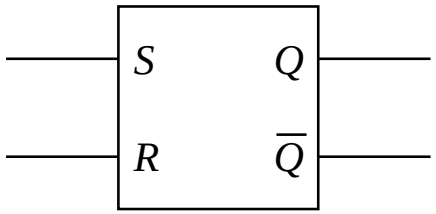


Disadvantages

- Short-Circuit currents destroy charge stored at X and Q
- For correct operation, ensure that $t_{riseCLK} < 5\ t_{c\text{-}q}$

Avoid Clock Overlap by using static SR FF



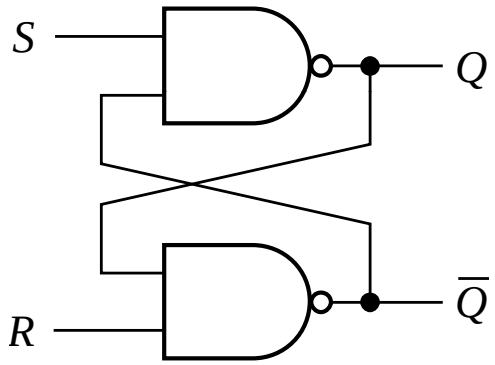


S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

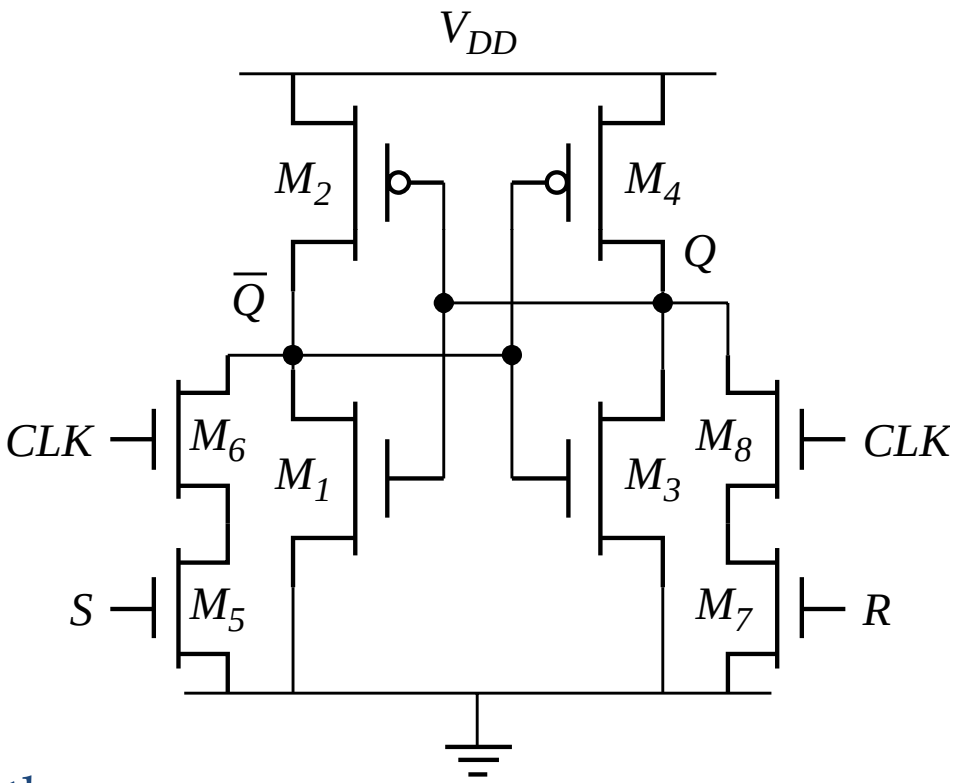
Forbidden State

Avoid Clock Overlap by using static SR FF

Cross-coupled NANDs

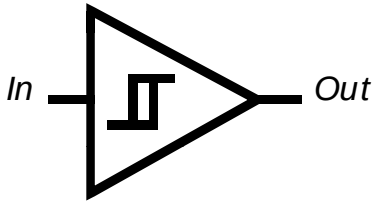


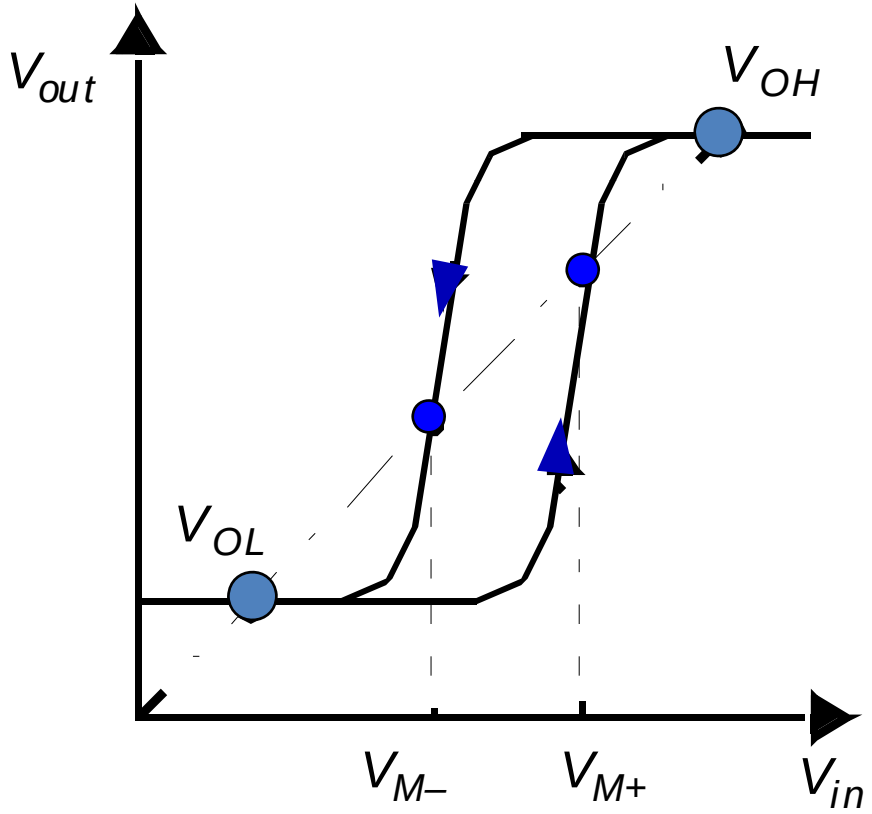
Added clock



This is not used in datapaths any more, but is a basic building memory cell

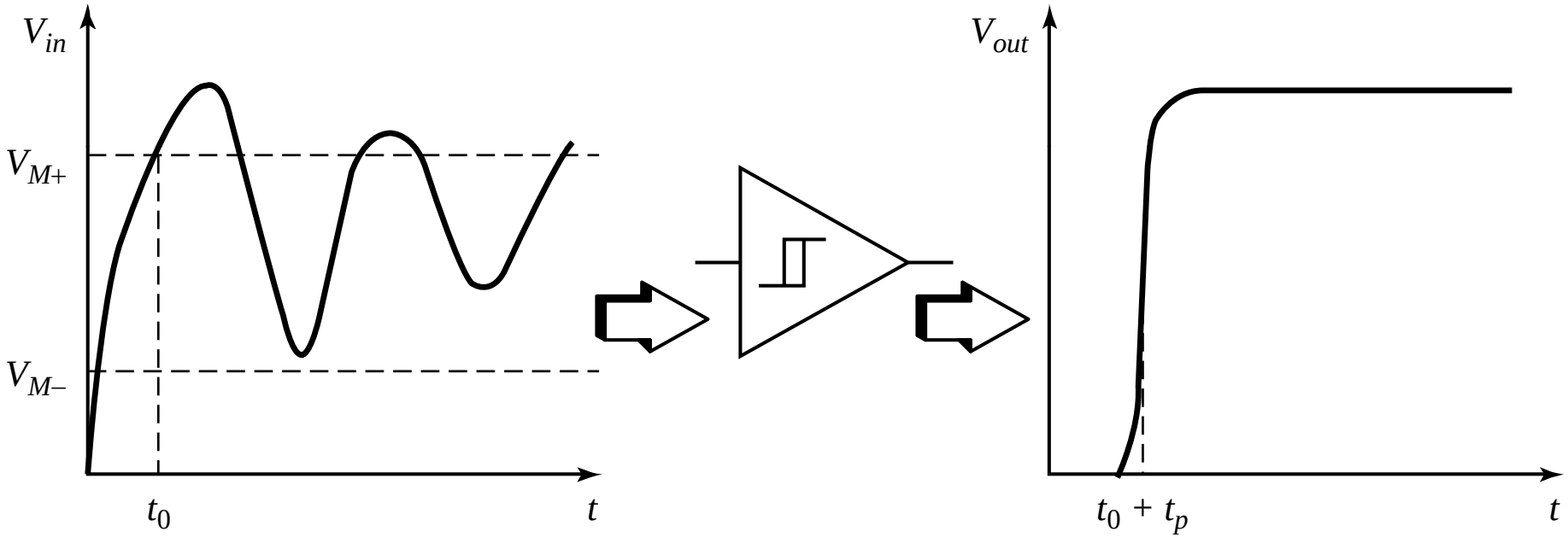
Non-Bistable Sequential Circuits—**Schmitt Trigger**



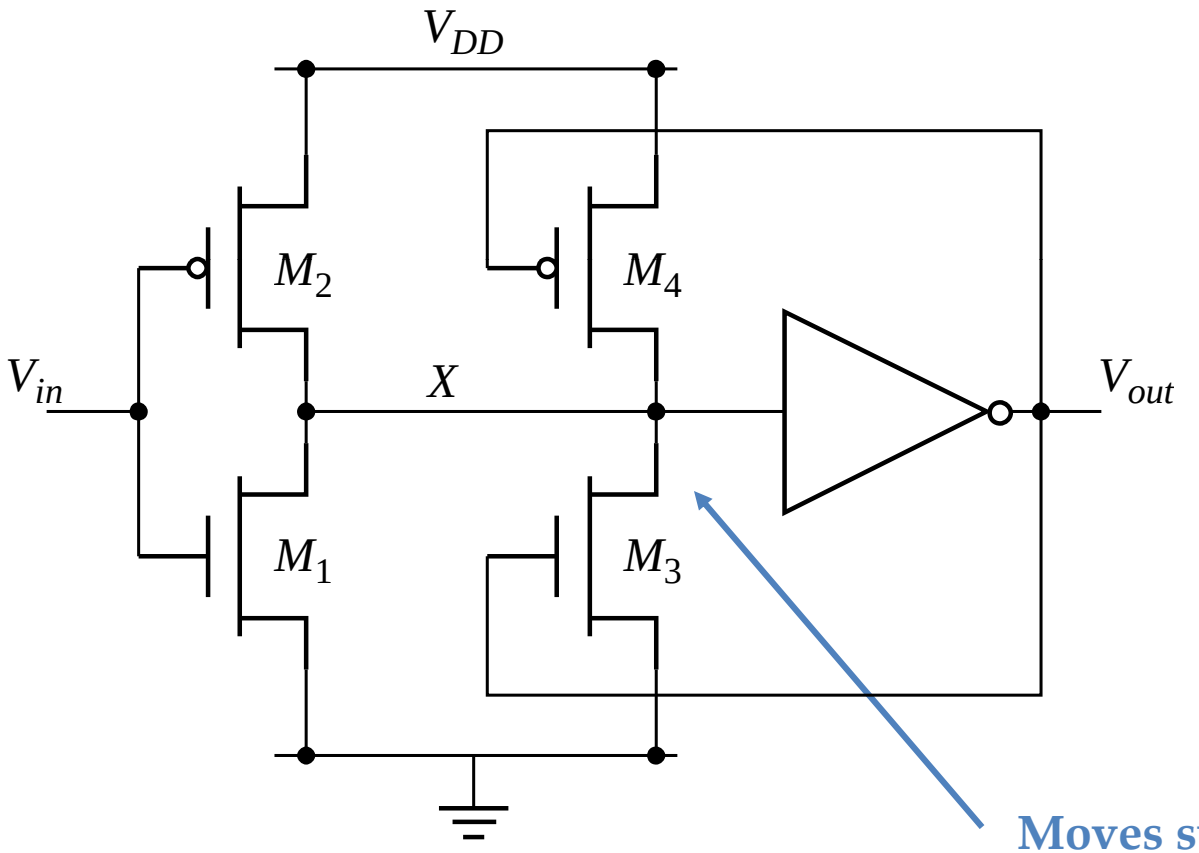


- **VTC with hysteresis**
- **Restores signal slopes**

Noise Suppression using Schmitt Trigger

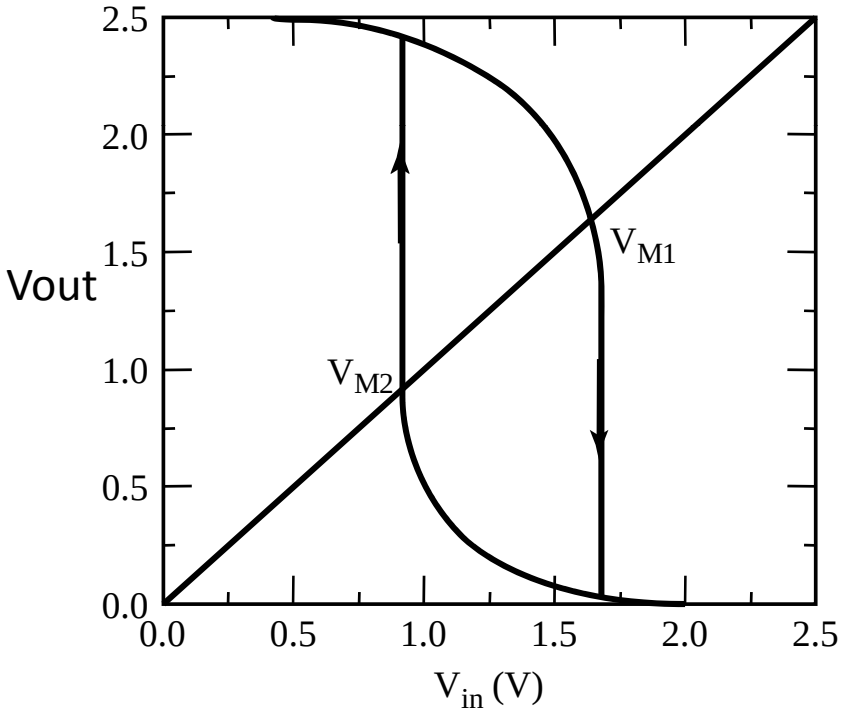


CMOS Schmitt Trigger

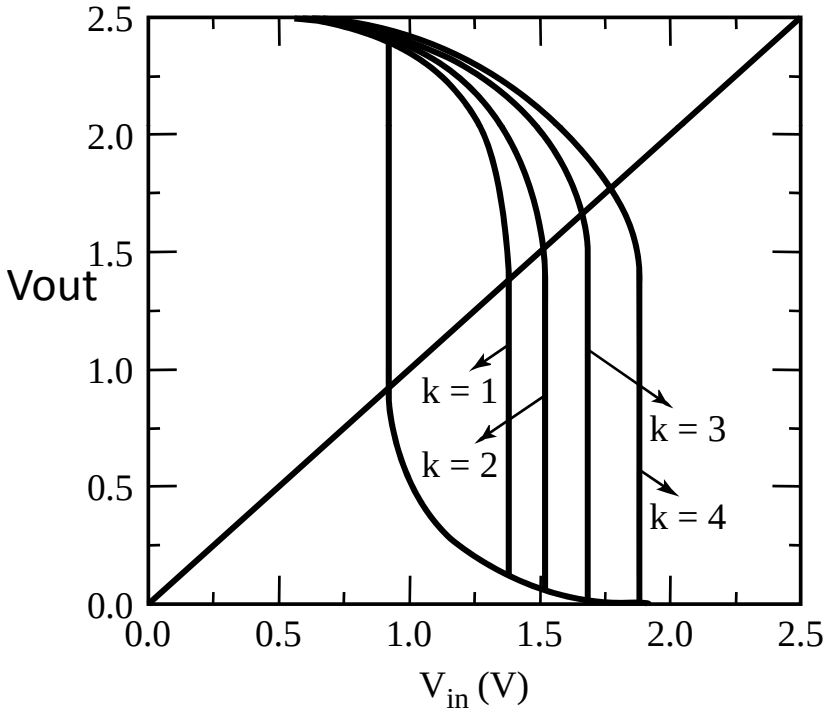


Moves switching threshold of the first inverter

Schmitt Trigger Simulated VTC



Voltage-transfer characteristics with hysteresis.



The effect of varying the ratio of the PMOS device M_4. The width is k* 0.5η m.

CMOS Schmitt Trigger (2)